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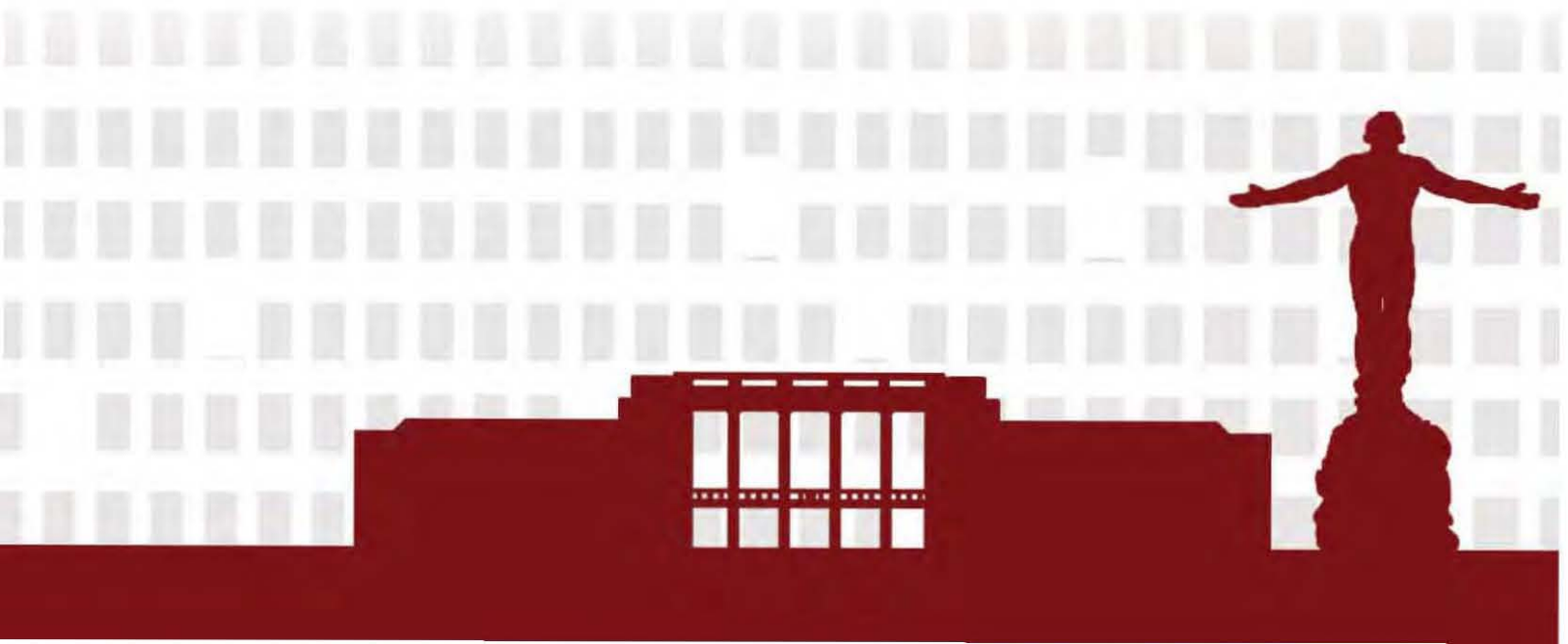
Metro Manila, Philippines



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A MODIFIED RF TO DC CONVERTER CMOS RECTIFIER DESIGN FOR ENERGY HARVESTING

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SUMMARY
This paper presents an enhanced CMOS based RF to DC converter design by modifying a published Voltage Multiplier circuit arrangement known as Mandal - Sarpehskar (MSVM) in order to provide a higher output voltage. This has been achieved by adding auxiliary PMOS and capacitor. A 4-stage Modified MSVM with each pumping capacitance of 10pF evaluated and implemented in TSMC 0.18um 1P6M 1.8V Logic Signal CMOS Technology. This design enhancement achieved a considerable increase of 0.5V at -5dBm in comparison to the conventional Mandal-Sarpeshkar. Also, it was observed that modified voltage multiplier shows higher conversion efficiency with the value of 11.53% in DC extraction from RF signal than the conventional MSVM design.

Keywords: Energy harvesting, RF to DC conversion, High frequency

Introduction

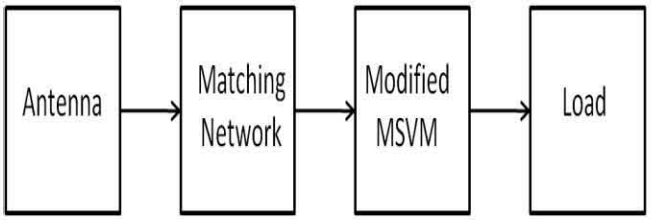
In recent years, development of technology is rapidly growing allowing the decrease of certain characteristics of a system or device like size and power consumption. However, these devices are powered by bulky batteries that need to be recharge or replace every so often. Extracting energy from the environment particularly RF signal is not only an eco-friendly way of generating free energy but can be a solution to minimize the consumption and usage of battery in most wireless devices. Developing efficient methods for extracting DC power from RF signals has become an important necessity for a number of applications involving self-powered devices and sensor nodes.

At its most basic, RFID systems consist of small transponders, or *tags*, attached to physical objects. RFID tags may soon become the most pervasive microchip in history. When wirelessly interrogated by RFID transceivers, or *readers*, tags respond with some identifying information that may be associated with arbitrary data records. Thus, RFID systems are one type of automatic identification system, similar to optical bar codes. Different RFID systems operate at a variety of radio frequencies. Each range of frequencies offers its own operating range, power requirements, and performance. Different ranges may be subject to different regulations or restrictions that limit what applications they can be used for [1].

In this work, an existing voltage multiplier named Mandal-Sarpeshkar Voltage Multiplier (MSVM) is modified by adding an auxiliary PMOS and capacitor to cancel the Vth effect which is imposing a limitation over the charge transferring capability of diode. Section 2 shows the circuit diagram of the work. Section 3 explains the different blocks of the circuit and the modifications made. The comparison of the proposed design with the conventional one is presented in section 4. Section 5 for the conclusion.

Circuit Design

Figure 1. shows the basic building blocks of a RF to DC Converter.



A simple mechanism on how the rectification process works; the antenna gathers or collects the ambient Radio Frequency, then the impedance matching networks boost the collected signals from the antenna to be able to turn on the transistors in the rectifier, then the rectifier converts the collected signal into a DC signal to be fed on the Load. In this work, a conventional voltage multiplier in the rectifier block was modified to achieve a higher voltage output.

Design Implementation

In the work of [2], a control mechanism is proposed for active MOS, which is capable in cancelling the V_{th} effect. In this paper, it is discussed that adding an auxiliary MOS and capacitor in the circuit of MSVM is a suitable approach to increase its output.

Figure 2 shows the conventional architecture of a MSVM. The operation of the four-transistor cell is easily understood if V_{rf+} and V_{rf-} are assumed to be large enough to turn the transistors on and off. The transistors then operate as switches. During half of the switching cycle, V_{rf+} is high and V_{rf-} is low. In this case N1 and P are on and N and P1 are off. Current flows through P's, named V_H and out through N1's, named V_L. During the other half of the cycle, N1 and P turn off and N and P1 are on, but the current flow at V_H and V_L has the same direction as before. Thus, a dc voltage is developed across a load connected between V_H and V_L. In general, $V_{DC} = (V_H - V_L) = (2V_{RF} - V_{drop})$, where V_{RF} is the ac voltage amplitude of V_{rf+} or V_{rf-} and V_{drop} represents losses due to switch resistance and reverse conduction [3].

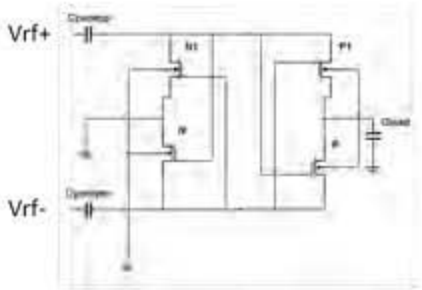


Figure 2. Conventional MSVM Nth stage.

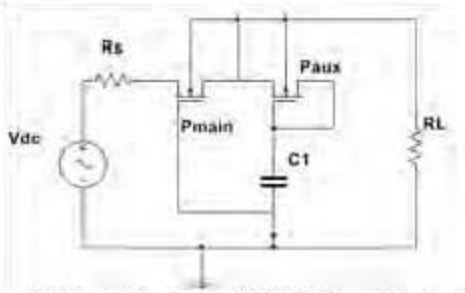


Figure 3. Modification of PMOS as Diode Circuit.

Figure 3 shows the modification of circuit as used in this paper. According to [2], this kind of architecture is capable of cancelling the threshold voltage of transistors, thus enhancing DC extraction ability.

Results And Discussions

The rectifier are implemented in CMOS 0.18 um technology. The width of PMOS (P_{main}), P_{aux} , and NMOS is selected t be 32 um, 1um and 20 um, respectively for maximum for DC voltage extraction. The capacitors (coupling and auxiliary) are kept at the value of 10pf and 1pf respectively. The pre simulation has been performed for both the MSVM and modified one consisting of 4 stages each at13.56 MHz. The resultant DC output voltage from both charge pumps, simulated for C_L = 10pf and R_L = 100kΩ is shown in Fig. 4.

As shown in Fig. 4, the modified Mandal-Sarpeshkar Voltage Multiplier displayed a higher output voltage compared to the conventional design. At maximum input power of 0 dBm, the Modified Mandal-Sarpeshkar Voltage achieved an output voltage of 3.7 V compared to the conventional one with only 2.38 V. While at minimum input power of -10 dBm, the Modified MSVM achieved an output voltage of 0.9V compared to the conventional one with only 0.7V. It displays an increase of about 1.5V to 0.5V from an input power of 0 dBm to -5 dBm.

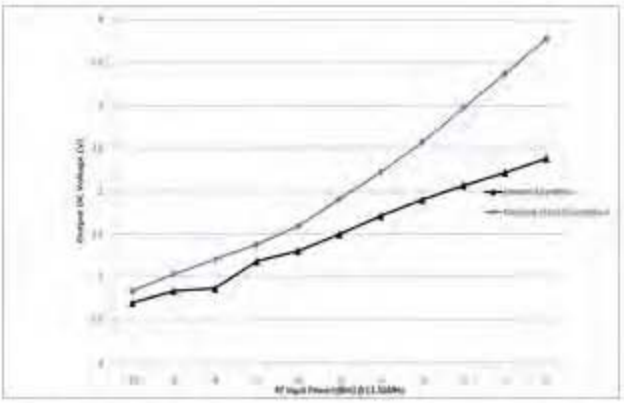


Figure 4. Measured Output Voltages of the RF to DC Converters.

Table 1 shows Specification summary of the Modified Mandal-Sarpeshkar Voltage Multiplier.

Table 1. Mandal-Sarpeshkar Voltage Multiplier Specifications

Technology	TSMC 0.18µm CMOS Process
Frequency	13.56 Mhz
Input Power Range	1000 – 100 µW
Output Voltage Range	0.83 – 3.78V
Load	100 KΩ
Conversion Efficiency	11.53%
No. of Stages	4
Chipa Area(Core)	768µm x 768 µm

It has been shown by simulations that the Modified Mandal-Sarpeshkar is capable of generating a higher output DC voltage over conventional one. By using 4 stages to compare the proposed circuit with the conventional Mandal-Sarpeshkar, it is shown that a considerable increase of 0.5V at -5dBm was achieved. It was found that proposed method is effective in generating a higher DC voltage as compared to conventional design.

Acknowledgments

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Reference

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